IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Timothy K. Carns, John L. Horvath, Lee J. DeBruler, and Michael J Westphal		
Assignee:	Zilog, Inc.		
Title:	PROCESS TO IMPROVE HIGH PERFORMANCE CAPACITOR PROPERTIES IN INTEGRATED MOS TECHNOLOGIES		
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COMMISSIONER FOR PATENTS
Washington, D. C. 20231

DECLARATION OF TIMOTHY K. CARNS

Sir:

I, Timothy K. Carns, declare as follows, under the penalty of perjury:

1. I am the co-applicant with John L. Horvath, Lee J. DeBruler, and Michael J Westphal of the above-identified patent application and have been an employee of Zilog Corporation, a company specializing in production of microprocessors and the Assignee of the above-identified application. I hold B.S., M.S., and Ph.D. degrees in Electrical Engineering, all from University of California at Los Angeles, and have worked for Zilog from 1994 until the present and currently hold the position of Director, Process Integration, Technology Development.

Supporting Documents

2. As part of our work for Zilog, John L. Horvath, Lee J. DeBruler, Michael J Westphal, and I developed processes to improve the performance of capacitors within an integrated MOSFET technology. These processes were all conceived prior to December 15, 1998, and diligently reduced to practice. This is described below with reference to Documents A-F, attached hereto:

Document A is a portion of a report presenting an analysis of experiments related to one of the embodiments of the present invention and was prepared by Lee J. DeBruler, Michael J Westphal, myself, and Suryanti Girlani, a junior level engineer who worked under my supervision on this project.

Document B is process flow runcard and presents the details of the processing related to the experiment reported in Document A. The originator of the request for this process flow was co-inventor Lee DeBruler and the request was authorized by me. Dates prior to December 15, 1998, have been removed from the submitted copy.

Documents C-F are related to two other embodiments of the present invention. Dates prior to December 15, 1998, have been removed from the submitted copies. Document C is a copy of the engineering notebooks of Suryanti Girlani, who was assigned by me to work on this project. These notebooks include notes of a meeting where the embodiments are presented followed by work compiling and analyzing the experiment performed under my direction.

Document D is a copy of notes of co-inventor Michael J Westphal from the same meeting where the embodiments are presented.

Document E is the process flow runcard for the experiments related to these embodiments. The originator of the request for this process flow was co-inventor Ms. Girlani and the request was authorized by me.

Document F are portions of reports presenting an analysis of experiments related to these embodiments and was prepared by Suryanti Girlani, Michael J Westphal, myself, and Lee J. DeBruler.

3. All of the foregoing documents have been kept among the usual business records of Zilog in the ordinary course of business.

Embodiments of the Invention

4. The original claims of the application presents three embodiments, a first embodiment found in claims 1-12, a second embodiment found in claims 13-25, and a third embodiment found in claims 26-30. The first embodiment is shown in Figures 2-5 of the application, the second embodiment is shown in Figures 6-9 of the application, and

the third embodiment is discussed with respect to Figure 2 starting on page 11, line 11 of the application. The third embodiment will be discussed first using Documents A and B and will be related to the base claim of this embodiment, claim 26. The first and second embodiments, related respectively to claims 1 and 13, will then be discussed with reference to Documents C-F. Claims 31-42 were added in an Amendment and are based on the first embodiment.

Reduction to Practice of the Third Embodiment

5. The third embodiment of the invention of the above referenced patent application presents a method for forming a capacitor where the lower electrode layer, inter-electrode dielectric layer, and upper electrode layer are formed. The upper electrode layer is then etched back to the dielectric layer to define the upper capacitor plates and expose a portion of the dielectric, while the dielectric and lower electrode layer are not yet defined. The resultant structure has the anti-reflective layer (ARL) formed upon it. The dielectric and lower dielectric are then etched, thereby forming the capacitor structure, following the formation of the ARL.

6. This process is described in Document A, a report dated 6 January, 1999, discussing a successful reduction to practice of this embodiment. In this document, and the other documents, L39 refers to the upper electrode layer and corresponds (after it has been etched) to reference number 140 Figures 2-9 of the application; it is also referred to as Poly 2 or P2 in various places. L40 refers to the lower electrode layer and corresponds to reference number 120 Figures 2-9 of the application; it is also referred to as Poly 1 or P1 in various places. The capacitor dielectric layer, corresponding to reference number 160, is variously referred to as IPD (inter-poly dielectric), oxide, ONO (oxide-nitride-oxide), or Novellus (a particular type of dielectric) in variations of the embodiments. The ARL is often referred to as PEARL (Plasma Enhanced ARL) since this is one preferred embodiment. Although in the context of another embodiment that is discussed below, pages 10 and 11 of Document C may be useful here for orientation purposes.

7. Document A is dated January 6, 1999, and presents an analysis of a successful reduction to practice as part of Lot D1549 of the third embodiment. Reference is also made to Lot D1114 where the ARL layer was applied after both the top electrode and

dielectric layer were etched at the "L39" etch, which resulted in the leakage described between the upper (poly 1) and lower (poly 2) electrodes that is described in more detail in the background section of the application. As described in the paragraph following the Objective of the report, the "experimental wafers had the IPD oxide removed at L40 etch prior to etching prior to etching poly 1"; that is, instead of etching the dielectric at the same time as the upper, poly 2 layer before the ARL is formed, the experimental wafers had the dielectric layer etched after the ARL layer is applied as part of the L40 etch for the lower, poly 1 layer. (This paragraph also refers to the use of spacers as found in the second embodiment discussed below.)

8. Data for the experimental wafers (wafers 8-10, 16-20, 23-25) are shown in Table 1 of the report. On the second included page of the report, noted as page 9 of 10, the successful reduction to practice of the third embodiment in these wafers from Lot D1549 is described. That is reduction to practice was performed in a diligent manner for Lot D1549 is shown in Document B.

9. The first page of Document B dates from prior to December 15, 1998, and is the "Special Test Request Form" to initiate the processing of Lot D1549. The originator of this request was a co-inventor, L. DeBruler, and my signature is under "TD Mgr" at the bottom. Beginning on page 3 of Document A (notated "sheet 1 of 30") is the process flow runcard for Lot D1549, as notated in the upper left corner. On the page notated "sheet 11 of 30", the lot is split into two groups as indicated by the notation "split lot into two groups for cap poly etch". The L40 etch of the third embodiment corresponding to "GROUP #2" as shown on sheet 12 of 30. The PEARL is deposited in the first line of "LOC 650" on sheet 13 of 30. Also note the parenthetical remark "NOTE WAFERS 3-5, 8-10, 13-15, 18-25 HAVE PEARL AND OXIDE OVER POLY 1" on this page.

10. The process flow runcard for the experimental wafers of this third embodiment continues with development prior to December 15, 1998. Steps for December 14, 1998, begin on sheet 21 of 30. These continue with daily entries from this date until January 11, 1999, subsequent to the report of a successful reduction to practice as described in Document A dated January 6, 1999, with only two gaps. A sheet of test data for tests conducted between December 21, 1998, and January 5, 1999, follows sheet 25 of 30.

11. The first of the two gaps occurs on sheet 22 of 30 where there are no entries between 12/15 and 12/18. This gap is notated "HOLD FOR JOHN HORVATH TO ETCH". (It also again contains the parenthetical notation of the wafers corresponding to the third embodiment.) John Horvath is one of the inventors of the above referenced application. Due to the special nature of the test chip being processed, the etch at this stage was to be conducted by Mr. Horvath. In order to develop the correct process recipe to ensure correct processing for this etch, test runs are required prior to running the actual wafers. This ensures that the previous processing steps do not need to be repeated and accounts for this first gap.

12. The second gap occurs on sheet 25 of 30 where there is a gap with no entries between 12/21 and 1-5. Referring to the "POST M1 Peval [process evaluation]" test request form on the next page, this shows that the wafers were undergoing the tests reported in Document A on December 21-24, 1998, and January 3-5, 1999. The remaining gap of December 25, 1998, to January 2, 1999, is a result of the Christmas, New Year shut down of the fabrication plant where this processing and testing was performed.

13. Therefore, the third embodiment of the above referenced patent application as reflected in claim 26 was conceived and diligence toward the January 6, 1999, reduction to practice began from a date prior to December 15, 1998.

Reduction to Practice of the First and Second Embodiments

14. The first embodiment of the invention of the above referenced patent application presents a method for forming a capacitor where the lower electrode layer, inter-electrode dielectric layer, and the upper electrode layer are formed. The upper electrode and dielectric layers are then etched back to the lower electrode layer to define the upper capacitor plate/dielectric structure and expose a portion of the lower electrode layer, while the lower electrode layer is yet defined. The resultant structure then has a conformal insulated layer formed upon it to cover the portion of the exposed dielectric between the defined upper electrode and lower electrode layer as shown in Figure 4 of the application, followed by etching the lower dielectric to form the capacitor structure.

15. In the second embodiment, after forming the lower electrode, dielectric, and upper electrode layers and defining the upper electrode, an insulating later is then formed of over the resultant structure. The insulating layer and dielectric layer are then etched to form side-wall spacers as shown in Figure 8 of the application.

16. Conception of the first and second embodiments prior to December 15, 1998, is shown in Documents C and D. The page number 1 of Document C and the single page of Document D are notes of a meeting prior to December 15, 1998. As noted in Document D, present at the meeting where myself, co-inventors John L. Horvath, Lee J. DeBruler, and Michael J Westphal, Suryanti Girlani, and others. Document D is the notes by Mr. Westphal. Document C contains pages from the engineering notebook of Ms. Girlani, an engineer assigned to compile and analyze the experiments related to these embodiments and working under my direction. (The numbering, "*i-iii*" and "1-61", is not original, but has been added for reference purposes.)

17. Beginning at "2:00 pm 7223/7235 ..." in the middle of the single page of Document D, the shortcomings of a prior art method of forming capacitors in the processing flow is noted along with possible solutions. The point noted "1" with "control 2" next to it corresponds to the third embodiment is described. The point noted "2" with "control 1" next to it corresponds to the process described in the Background section of the above referenced application. The point noted "8", "seal edge with RTP or dep/spacer etch" describes the additions to the prior art found in the first and second embodiments, RTP standing for rapid thermal process that is a particular embodiment for forming the conformal insulating layer.

18. Page 1 of Document C also is from this meeting. Under "Solutions" at "1", embodiment 3 is described "don't remove IPD at L39" and reference made to lot 1549 discussed above. At "2", a drawing shows the structure resultant using the process described in the Background section of the above referenced application showing the undercut of the "IPD Removal at L39". At "8", the first and second embodiment are described by "Seal edge w/RTP or Dep/Spacer" and an adjacent sketch of forming the spacers of the second embodiment. Subsequent pages of Document C proceed to develop and analyze the experiment to reduce the invention to practice, starting from before December 15 until the experiment was submitted.

19. On page 2 of Document C are the notes beginning the compilation of the experiment and review of the problem. On page 2, near bottom under "Factor" is "Edge Seal" with the corresponding action of "RTP, Spacer (deposition & spacer etch)". The preparation work continues with evaluation of the problem as it appears in Lot D1114 discussed above in the third paragraph of the third section. Note the reference to "Work on D1114 PEVAL [Process EVALuation] Summary report" on pages 4 and 5 followed by several pages of analysis. At the top of page 8, reference is made to reviewing the split list of several wafer lots, including Lot D1549 of the third embodiment discussed in Documents A and B.

20. In these documents, "splits" refer to the variation done on the inputs in the experiment. For example, Sheet 9 of 20 on the D1549 runcard of Document B shows "splits" for the capacitor oxide where one group of wafers gets a deposited oxide while the other group gets a grown oxide. A split list is the compilation of all splits done in a given experiment, such as that shown on page 2 of Document E.

21. The pages before page 9 of Document C are all work prior to December 15, 1998, analyzing the problem in light of what will be the control for the experiment. Page 9 begins the entries from December 15, 1998. Beginning with page 9, the analysis that results in the requested experiment begins.

22. On page 11 is a set of figures showing the third embodiment as discussed above, followed by several pages of analysis. The relevance of this background work and why it forms part of a diligent reduction to practice is presented on page 15 in the paragraph beginning "The last couple of days...". In these comments, reference is made to several lots: D1549 is the lot discussed in Documents A and B for the third embodiment that will serve as the second control; D1261 is another lot that had an experiment similar to that done on D1549 to look at the third embodiment: and D1168 is another experiment which investigated different capacitor dielectrics, including oxide-nitride-oxide, nitrided oxide, and others, with the hope of improving capacitor performance. On page 18 is a proposed split list for the experiment for the design of the experiment, which the following page notes was sent to Mr. Horvath, Mr. Westphal, and myself.

23. The engineering notes of Document C by Ms. Girlani continue until January 6, 1999, with relevant entries for every day, except as noted. The first gap is a lack of entries for December 19 and 20, 1998, which were a Saturday and Sunday. In the entries for December 23, 1998, on page 31, reference is made to a meeting on the previous day with Mr. Westphal ("Mike") and myself to discuss the split list for the experiment. This page and the next few pages have a number of sketches showing the first and second embodiments of the above referenced application. There is another gap for the dates of December 24-29, 1998, between pages 33 and 34 due to the Christmas holiday. The notes resume on page 34 with a meeting with Mr. Westphal, myself, and several others. (Lot D1315 had the PEARL removed to verify that this layer contributed to the leakage between the capacitor plates. Wafers 15, 20, and 25mentioned both in this location and again on page 52 of this document were the wafers that did not have the PEARL.)

24. On page 36, reference is made to the "Z37223 list"; Z37223 was the number assigned to the process flow for experiment that reduced the first and second embodiments to practice, as discussed below. At the top of page 40 is reference to a meeting to review the experiment. There is a gap between pages 46 and 48 on January 1-3 due to the New Year holiday and that the second and third were a Saturday and Sunday. On the notes for January 4, 1999, beginning on page 48, is reference to a meeting at which all of the inventors plus several others were to be present, followed by a presentation of what was to be presented on the next few pages. This is followed by a review of the meeting.

25. In the middle of page 54 is reference to a review of the run-card that will be followed by the experiment and which Mr. Horvath and myself, among others, were present. The corresponding split list is on the following pages. Document C ends with the January 6, 1999, entry of page 61.

26. Document E is the log from the manufacturing line of the experiment run to validate the first and second embodiments that had been assigned process flow number Z37223. As shown on the Request of page 1, this was assigned lot number E0034. The originator of this request was Ms. Girlani and my signature is under "TD Mgr" at the bottom. The appropriate approvals were obtained on January 7 and 8, 1999. The second and third page of Document E are the split list for the flow and are the same as those

found on page 55 and 56 of Document C. In particular note the points under "Questions to be answered" that describe both the problem and the first and second embodiments.

27. The subsequent pages of Document E present the log entries from the manufacturing line for flow Z37223 on lot E0034, as noted in the upper left corner. The various processing stages are dated from January 8, 1999, to February 21, 1999, with only the noted gaps. On sheet 7 of 38, there is a gap for January 14, 1999, with the notation "DIRECT TRANSFER TO AMORPHOUS SI DEPEOSITION", due to tool availability. The processing continued once the appropriate apparatus was available. Beginning on sheet 10 of 38, the wafer are separated into the different groups; for example, note that on sheet 15 of 38, a set of wafers do not receive spacers. There is another gap for the dates of January 23 and 24, 1999, in order to develop the correct process recipe to ensure correct processing for this etch. There are then gaps on the dates of February 7 and 10, as seen on sheet 32 of 38, due to tool availability and on February 15-17, as seen on sheet 36 of 38, when the CVD TiN system needed for the next step was down for repair.

28. Document E ends with a "P-EVAL REQUEST FORM" for the tests to evaluate the process of Lot E0034. These tests occurred on February 22-25, 1999, and show that there was a successful reduction to practice, as discussed in Document F. Document F presents some key pages from summary reports on Lot E0034 processed according flow 37223 based on the tests.

29. The first page of Document F is from a Report dated March 25, 1999, by S. Girlani (whose engineering notebook was the source of Document), myself, and co-inventors M. Westphal and L. DeBruler. This report was concerned specifically with Lot E0034 processed according flow 37223. The Executive Summary presents the problem addressed by the experiment, namely capacitor leakage. Under point 1, the implementation of spacers (the second embodiment) is discussed and considered successful. Under point 2, the first embodiment with the conformal insulating layer formed in a rapid thermal process (RTP) is discussed on considered successful.

30. Document F also presents the executive summary and conclusions from a report by myself dated April 2, 1999. This report is related to capacitor performance and in particular refers to results of Lot E0034. This report concerns not just the material of

the report dated March 25, but also the formation of capacitors in the larger context of an actual product. The first and second embodiments are presented in the Introduction. In the conclusion, it is recommended that the first embodiment be incorporated into the flow that was to be used for the actual product.

31. Therefore, the first and second embodiments of the above referenced patent application as respectively reflected in claims 1 and 13 were conceived and diligence to actually reduce them to practice began prior to December 15, 1998.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Executed this 14th day of September, 2001, at Nampa, Idaho.

Timothy K. Carns